Journal of the European Ceramic Society 19 (1999) 1413-1415

PII: S0955-2219(98)00447-6
0955-2219/99/$ - see front matter

A Novel Integrated Thin Film Capacitor Realized by a Multilayer Ceramic–Electrode Sandwich Structure

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Abstract

In this work a method will be presented to increase the capacitance of an integrated capacitor per chip area using a sandwich multilayer structure, which is successfully employed for ceramic multilayer capacitors used as surface mount devices. On a Pt coated Si/SiO_2 wafer polycrystalline $SrTiO_3$ films deposited by a chemical solution deposition (CSD) method and sputter deposited Pt layers have been alternatingly arranged. Connecting all even Pt electrode layers and all odd, respectively, leads to an equivalent circuit of several high permittivity $SrTiO_3$ thin film capacitors in parallel. © *1999 Elsevier Science Limited. All rights reserved*

Keywords: integration, films, $BaTiO_3$ and titanates, capacitors.

1 Introduction

The progress of further reduction of the structure size for integrated circuits requires new approaches for the integrated devices. Integrated monolayer capacitors with a dielectric (Ba,Sr)TiO_3 (BST) thin film prepared by simple CSD technique have already been put into mass-production of e.g. MMICs.[1,2] The obvious advantages of placing the capacitors on-chip are the reduction in system size and the reduction of parasitic circuit inductance due to the reduction of the number of pins. The aim of this trend is to achieve a maximum capacitance per chip area.

With the design of the integrated capacitor presented in this paper we intend to achieve the highest possible capacitance per chip area. Therefore, a design was applied with alternatingly arranged dielectric and electrode layers, which leads to an equivalent circuit of several capacitors in parallel. This design is also successfully employed for Ceramic Multilayer Capacitors (MLC) used as surface mount devices. Additionally, the integrated capacitor was deposited on a SiO_2 substrate, which is compatible to the substrates used in the semiconductor industry.

Recently, first Thin Film Multilayer Capacitors (TMC) have been realized with BST thin films deposited by Metal–Organic CVD on a MgO single crystal substrate with Pt electrodes[3] (Fig. 1).

2 Experimental

For the dielectric layer, high permittivity $SrTiO_3$ thin films were prepared by a CSD technique using strontium-propionate dissolved in propionic acid and 1-butanol mixed with titanium-tetra-n-butoxide, stabilized by adding acetylacetone. After multiple deposition steps and crystallization of each layer(at 650°C for 30 min in O_2) the $SrTiO_3$ films underwent a final crystallization treatment (at 700°C for 1 h in O_2). The platinum electrodes were sputter-deposited with a shadow mask using a magnetron sputtering system.

In Fig. 2 processing of the TMC is sketched: After $SrTiO_3$ deposition [Fig. 2(a)] on a platinized Si/SiO_2 wafer with a TiO_x, adhesion layer underneath the Pt bottom electrode the first intermediate Pt electrode layer was sputter-deposited [Fig. 2(b)]. After the deposition of the second dielectric layer [Fig. 2(c)] a contact hole was wet-chemically etched [Fig. 2(d)] to connect the bottom electrode to the intermediate electrode, which was deposited in the following step [Fig. 2(e)]. The steps of electrode and dielectric layer deposition and etching of the contact hole were subsequently repeated until the TMC consisted of at least three dielectric and four electrode layers [Fig. 2(f)–(h)].

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3 Results and Discussion

The $SrTiO_3$ films used as dielectric layer had a thickness of approximately 300 nm. The permittivity of the film at room temperature was determined to approximately 180 and the leakage current at 125°C and 3 V was below 10^{-6} A cm^{-2}. X-ray diffraction measurements (XRD) revealed the films to be polycrystalline and phase pure [Fig. 3(a)]. From atomic force micrographs (AFM) the average surface roughness was determined to $R_A = 1{\cdot}4$ nm with a standard deviation of RMS = 1·8 nm [Fig. 3(b)] for a scanned area of $5\times5\,\mu m^2$.

In Fig. 4(a) a schematic cross section of a TMC with four electrode layers is shown and the corresponding SEM micrograph can be seen in Fig. 4(b). Additionally, the effective capacitance area and the total area of the TMC are introduced. Figure 5(a) and (b) shows a schematic top view and a micrograph of the TMC, respectively. Again, the effective capacitance area and the total area are indicated. One advantage of this design is the good

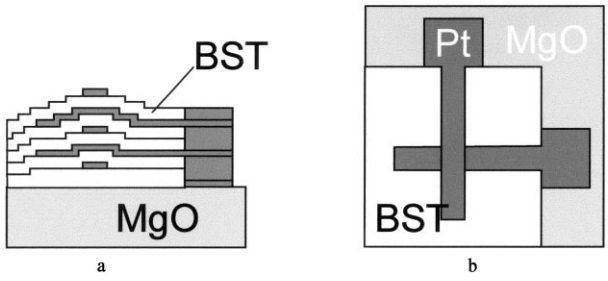

Fig. 1. BST thin film multilayer capacitor deposited by MOCVD with Pt electrodes on MgO substrate recently reported by Takeshima *et al.*[3]

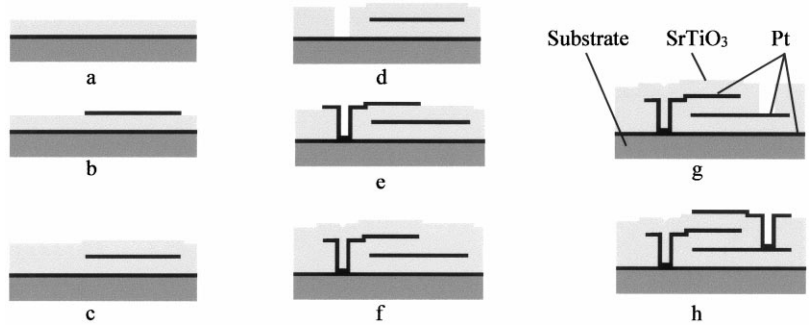

Fig. 2. Processing of the TMC: (a) sputter deposition of the Pt bottom electrode on a Ti/TiN adhesion layer and subsequently the dielectric $SrTiO_3$ deposition; (b) Pt electrode deposition; (c) deposition of the second $SrTiO_3$ layer; (d) wet-chemically etching of the contact hole; (e) Pt electrode deposition; (f) deposition of the third $SrTiO_3$ layer; (g) see (d); (h) see (e).

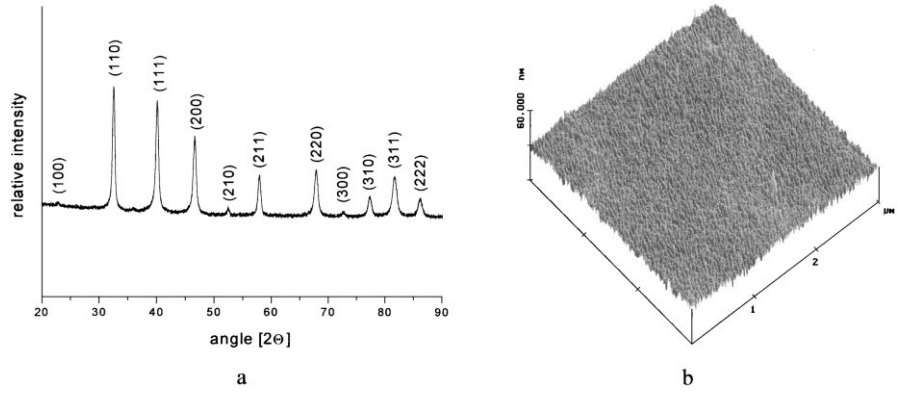

Fig. 3. (a) XRD measurement and (b) AFM measurement of $SrTiO_3$ thin film (300 nm) used for the TMC structure.

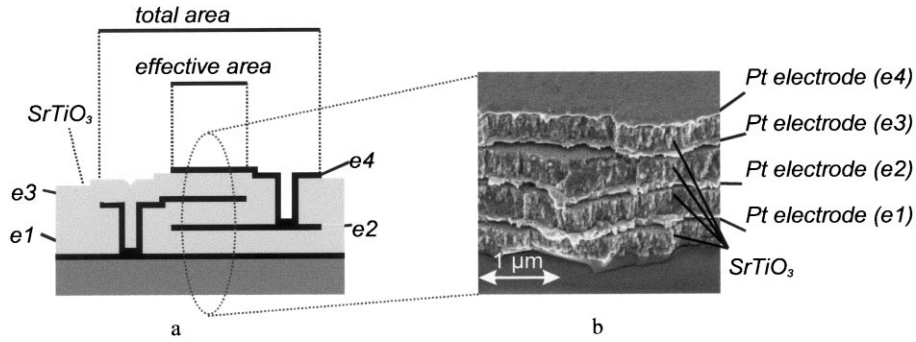

Fig. 4. (a) Schematic cross section (not to scale) of a TMC with three dielectric and four electrode layers (e1...e4) and introduction of the effective and total capacitor area; (b) the corresponding SEM micrograph.

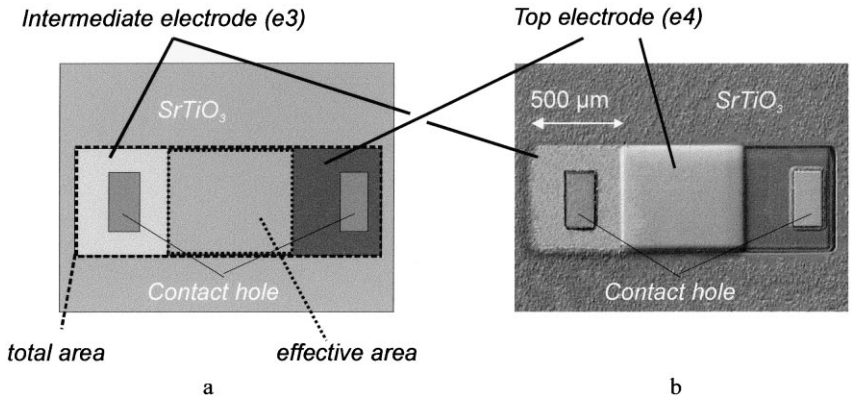

Fig. 5. (a) Schematic top view and (b) micrograph of the top view of a TMC.

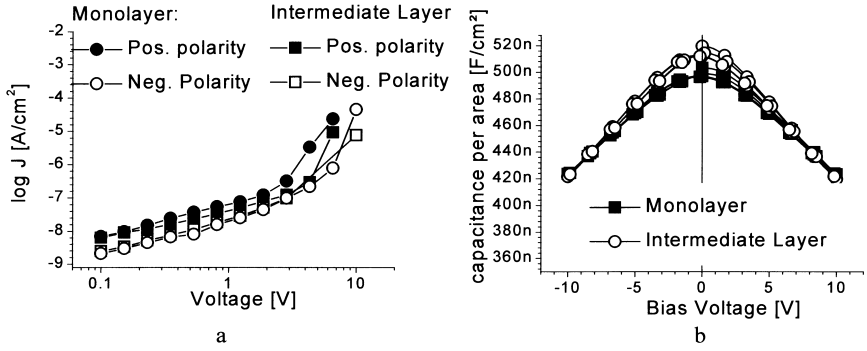

Fig. 6. (a) J–V characteristic at 125°C of a monolayer $SrTiO_3$ thin film ($t = 300$ nm, measured between el and e2, open symbols) and an intermediate layer ($t = 300$ nm, between e2 and e3); (b) C–V characteristic at room temperature of a monolayer and an intermediate layer $SrTiO_3$ film.

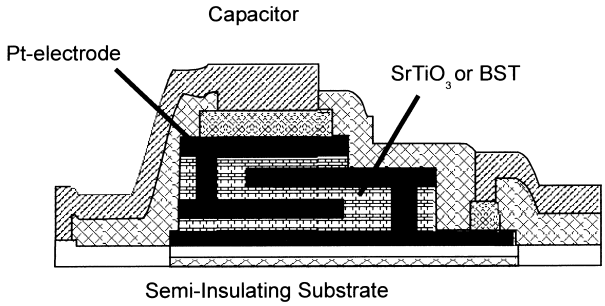

Fig. 7. Possible future application of the TMC structure as decoupling or bypass capacitor in ICs.

ratio between the effective capacitance area and the total area (>40% for a total area of 0·725 mm^2). With this TMC design a further reduction of the capacitor size seems feasible. J–V and C–V characteristics [Fig. 6(a) and (b)] reveals no significant difference between a monolayer capacitor [measured between electrodes el and e2, see Fig. 4(a)] and an intermediate capacitor (between e2 and e3).

4 Summary

A method has been presented to increase the capacitance per area for integrated capacitors using a thin film multilayer (TMC) structure. The TMC structure has been deposited on a platinized Si/SiO_2 substrate, which is a standard semiconductor substrate. The design of the TMC is scalable, i.e. a further reduction of the feature size seems achievable. The TMC design exhibits a good ratio of the effective capacitance area to the total area required for the TMC (>40%, for a total area of 0·725 mm^2). A possible future application of the TMC is the use as decoupling or bypass capacitor in ICs as sketched in Fig. 7.

Acknowledgements

The authors would like to thank Dr K. Szot for his assistance in conducting the AFM measurements, Dr U. Schnakenberg for many fruitful discussions and R. Gerhardt for preparing the $SrTiO_3$ thin films.

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